S70FL256P

256-Mbit 3.0V Flash

This product is not recommended for new and current designs. For new and current designs, the S25FL256S supersedes S70FL256P. This is the factory-recommended migration path. Refer to the S25FL256S datasheet for specifications and ordering information, and AN98592 for changes required to migrate from existing designs based on S70FL256P.

Distinctive Characteristics

Architectural Advantages

- Single Power Supply Operation
  - Full voltage range: 2.7 to 3.6V read and write operations
- Memory Architecture
  - Uniform 64 kB sectors
    - Top or bottom parameter block (Two 64-kB sectors broken down into sixteen 4-kB sub-sectors each) for each Flash die
  - Uniform 256 kB sectors (no 4-kB sub-sectors)
  - 256-byte page size
- Program
  - Page Program (up to 256 bytes) in 1.5 ms (typical)
  - Program operations are on a page by page basis
  - Accelerated programming mode via 9V W#/ACC pin
  - Quad Page Programming
- Erase
  - Bulk erase function for each Flash die
  - Sector erase (SE) command (D8h) for 64 kB and 256 kB sectors
  - Sub-sector erase (P4E) command (20h) for 4 kB sectors (for uniform 64-kB sector device only)
  - Sub-sector erase (P8E) command (40h) for 8 kB sectors (for uniform 64-kB sector device only)
- Cycling Endurance
  - 100,000 cycles per sector typical
- Data Retention
  - 20 years typical
- Device ID
  - JEDEC standard two-byte electronic signature
  - RES command one-byte electronic signature for backward compatibility
- One-time programmable (OTP) area on each Flash die for permanent, secure identification; can be programmed and locked at the factory or by the customer
- CFI (Common Flash Interface) compliant; allows host system to identify and accommodate multiple flash devices
- Process Technology
  - Manufactured on 0.09 µm MirrorBit® process technology
- Package Option
  - Industry Standard Pinouts
  - 16-pin SO package (300 mils)
  - 24-ball BGA (6 × 8 mm) package, 5 × 5 pin configuration

Performance Characteristics

- Speed
  - Normal READ (Serial): 40 MHz clock rate
  - FAST_READ (Serial): 104 MHz clock rate (maximum)
  - DUAL I/O FAST_READ: 80 MHz clock rate or 20 MB/s effective data rate
  - QUAD I/O FAST_READ: 80 MHz clock rate or 40 MB/s effective data rate
- Power Saving Standby Mode
  - Standby Mode 160 µA (typical)
  - Deep Power-Down Mode 6 µA (typical)

Memory Protection Features

- Memory Protection
  - W#/ACC pin works in conjunction with Status Register Bits to protect specified memory areas
  - Status Register Block Protection bits (BP2, BP1, BP0) in status register configure parts of memory as read-only

Software Features

- SPI Bus Compatible Serial Interface

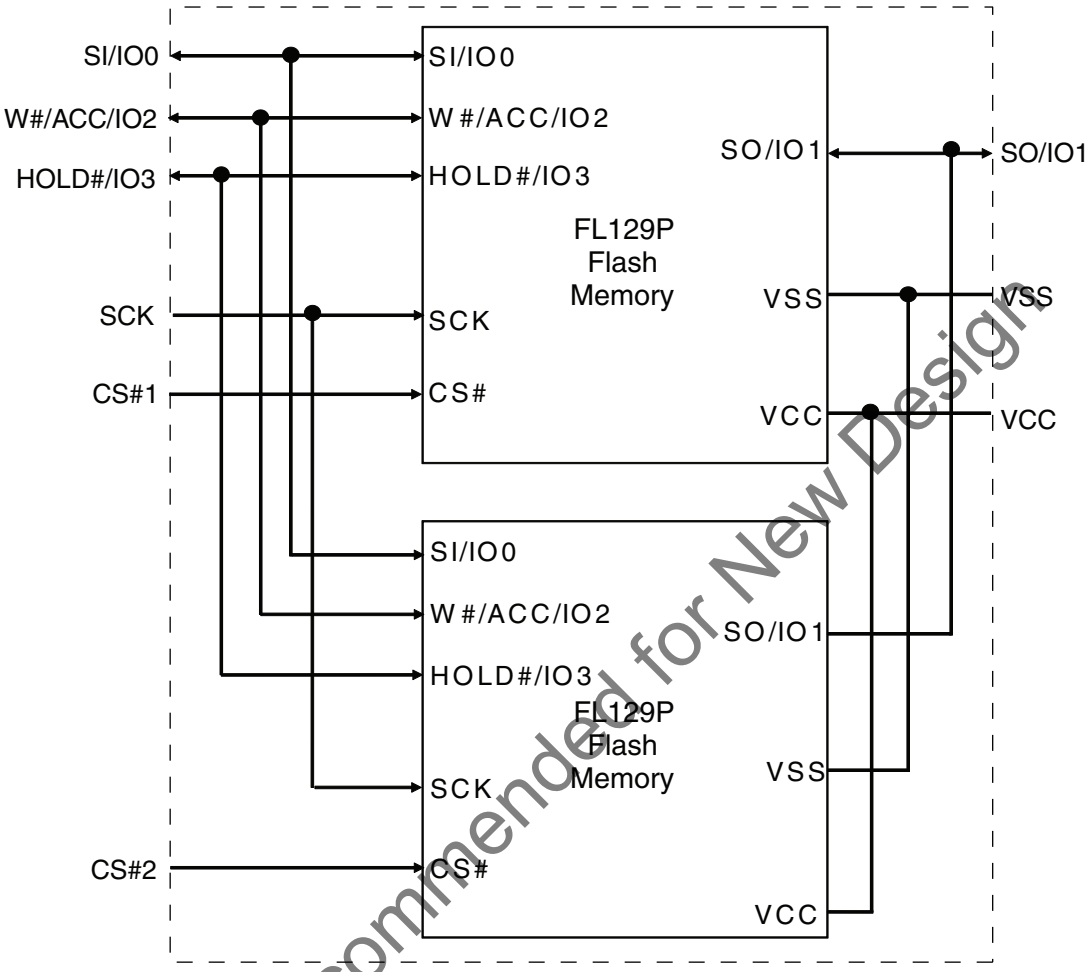
General Description

This document contains information for the S70FL256P device, which is a dual die stack of two S25FL129P die. For detailed specifications, refer to the discrete die datasheet.

Document Name	Cypress Document Number
S25FL129P, 128-Mbit 3.0V Flash Memory Datasheet	002-00648

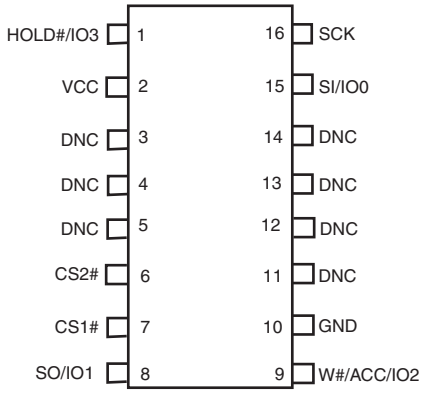
Contents

1. Block Diagram



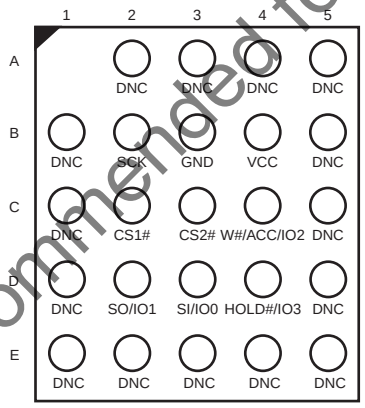
2. Connection Diagrams

Figure 2.1 16-pin Plastic Small Outline Package (SO)



Note:
DNC = Do Not Connect (Reserved for future use)

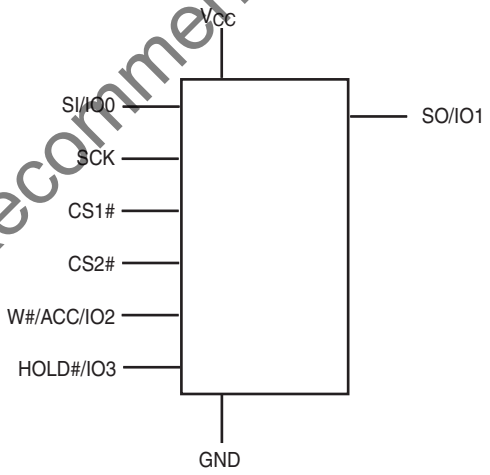
Figure 2.2 6 x 8 mm 24-ball BGA Package, 5 x 5 Pin Configuration



3. Input/Output Description

Signal	I/O	Description
SO/IO1	I/O	**Serial Data Output**: Transfers data serially out of the device on the falling edge of SCK. Functions as an I/O pin in Dual and Quad I/O, and Quad Page Program modes.
SI/IO0	I/O	**Serial Data Input**: Transfers data serially into the device. Device latches commands, addresses, and program data on SI on the rising edge of SCK. Functions as an I/O pin in Dual and Quad I/O mode.
SCK	Input	**Serial Clock**: Provides serial interface timing. Latches commands, addresses, and data on SI on rising edge of SCK. Triggers output on SO after the falling edge of SCK.
CS1# CS2#	Input	**Chip Selects**: Places one of the Flash die in active power mode when driven low. Deselects Flash die and places SO at high impedance when high. After power-up, device requires a falling edge on CS1# and CS2# before any command is written. Device is in standby mode when a program, erase, or Write Status Register operation is not in progress.
HOLD#/IO3	I/O	**Hold**: Pauses any serial communication with the device without deselecting it. When driven low, SO is at high impedance, and all input at SI and SCK are ignored. Requires that CS1# or CS2# also be driven low. Functions as an I/O pin in Quad I/O mode.
W#/ACC/IO2	I/O	**Write Protect**: Protects the memory area specified by Status Register bits BP2:BP0. When driven low, prevents any program or erase command from altering the data in the protected memory area. Functions as an I/O pin in Quad I/O mode.
V_{CC}	Input	**Supply Voltage**
GND	Input	**Ground**

4. Logic Symbol



5. Device Operations

5.1 Programming

Each Flash die must be programmed independently due to the nature of the dual die stack.

5.2 Simultaneous Die Operation

The user may only access one Flash die of the dual die stack at a time via its respective Chip Select.

5.3 Sequential Reads

Sequential reads are not supported across the end of the first Flash die to the beginning of the second. If the user desires to sequentially read across the two die, data must be read out of the first die via CS1# and then read out of the second die via CS2#.

5.4 Sector/Bulk Erase

A sector erase command must be issued for sectors in each Flash die separately. Full device Bulk Erase via a single command is not supported due to the nature of the dual die stack. A Bulk Erase command must be issued for each die.

5.5 Status Register

Each Flash die of the dual die stack is managed by its own Status Register. Reads and updates to the Status Registers must be managed separately. It is recommended that Status Register control bit settings of each die are kept identical to maintain consistency when switching between die.

5.6 Configuration Register

Each Flash die of the dual die stack is managed by its own Configuration Register. Updates to the Configuration Register control bits must be managed separately. It is recommended that Configuration Register control bit settings of each die are kept identical to maintain consistency when switching between die.

5.7 Block Protection

Each Flash die of the dual die stack will maintain its own Block Protection. Updates to the TBPROT and BPNV bits of each die must be managed separately. By default, each die is configured to be protected starting at the top (highest address) of each array, but no address range is protected. It is recommended that the Block Protection settings of each die are kept identical to maintain consistency when switching between die.

6. Read Identification (RDID)

The Read Identification (RDID) command outputs the one-byte manufacturer identification, followed by the two-byte device identification and the bytes for the Common Flash Interface (CFI) tables. Each die of the FL256P dual die stack will have identical identification data as the FL129P die, with the exception of the CFI data at byte 27h, as shown in Table 6.1.

Table 6.1 Product Group CFI Device Geometry Definition

Byte	Data	Description
27h	19h	Device Size = 2^N byte

7. DC Characteristics

This section summarizes the DC Characteristics of the device. Designers should check that the operating conditions in their circuit match the measurement conditions specified in the Test Specifications in Table 8.1 on page 8, when relying on the quoted parameters.

Table 7.1 DC Characteristics (CMOS Compatible)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ. (1)	Max.	
V_{CC}	Supply Voltage	–	2.7	–	3.6	V
V_{HH}	ACC Program Acceleration Voltage	V_{CC} = 2.7V to 3.6V	8.5	–	9.5	V
V_{IL}	Input Low Voltage	–	–0.3	–	0.3 x V_{CC}	V
V_{IH}	Input High Voltage	–	0.7 x V_{CC}	–	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA, V_{CC} = V_{CC} min.	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.1 mA	V_{CC} - 0.6	–		V
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND	–	–	±2	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND	–	–	±2	µA
I_{CC1}	Active Power Supply Current - READ (SO = Open)	At 80 MHz (Dual or Quad)	–	–	44	mA
		At 104 MHz (Serial)	–	–	32	
		At 40 MHz (Serial)	–	–	15	
I_{CC2}	Active Power Supply Current (Page Program)	CS# = V_{CC}	–	–	26	mA
I_{CC3}	Active Power Supply Current (WRR)	CS# = V_{CC}	–	–	15	mA
I_{CC4}	Active Power Supply Current (SE)	CS# = V_{CC}	–	–	26	mA
I_{CC5}	Active Power Supply Current (BE) (2)	CS# = V_{CC}	–	–	26	mA
I_{SB1}	Standby Current	CS# = V_{CC}; SO + V_{IN} = GND or V_{CC}	–	160	500	µA
I_{PD}	Deep Power-down Current	CS# = V_{CC}; SO + V_{IN} = GND or V_{CC}	–	6	20	µA

Notes:

1. *Typical values are at T_{AI} = 25°C and V_{CC} = 3V.*
2. *Bulk Erase is on a die per die basis, not for the whole device.*

8. Test Conditions

Figure 8.1 AC Measurements I/O Waveform

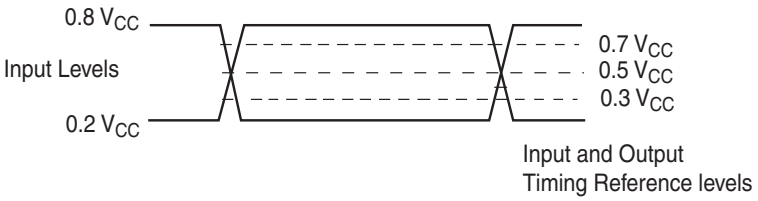


Table 8.1 Test Specifications

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times (1)		5	ns
	Input Pulse Voltage	0.2 V_{CC} to 0.8 V_{CC}		V
	Input Timing Reference Voltage	0.3 V_{CC} to 0.7 V_{CC}		V
	Output Timing Reference Voltage	0.5 V_{CC}		V

Note:
1. Input rise and fall times are 0-100%.

9. AC Characteristics

Table 9.1 AC Characteristics

Symbol (Notes)	Parameter (Notes)	Min. (Notes)	Typ (Notes)	Max (Notes)	Unit
f_R	SCK Clock Frequency for READ command	DC	–	40	MHz
	SCK Clock Frequency for RDID command	DC	–	50	MHz
f_C	SCK Clock Frequency for all others: FAST_READ, PP, QPP, P4E, P8E, SE, BE, DP, RES, WREN, WRDI, RDSR, WRR, READ_ID	DC	–	104 (serial) 80 (dual/quad)	MHz
t_{WH}, t_{CH} (5)	Clock High Time	4.5	–	–	ns
t_{WL}, t_{CL} (5)	Clock Low Time	4.5	–	–	ns
t_{CRT}, t_{CLCH}	Clock Rise Time (slew rate)	0.1	–	–	V/ns
t_{CFT}, t_{CHCL}	Clock Fall Time (slew rate)	0.1	–	–	V/ns
t_{CS} (9)	CS# High Time (Read Instructions) CS# High Time (Program/Erase)	10 50	–	–	ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3	–	–	ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	3	–	–	ns
$t_{SU:DAT}$	Data in Setup Time	3	–	–	ns
$t_{HD:DAT}$	Data in Hold Time	2	–	–	ns
t_V	Clock Low to Output Valid	0	–	9 (Serial)Δ 10.5 (Dual/Quad)Δ 7.8 (Serial)∞ 9 (Dual/Quad)∞	ns
t_{HO}	Output Hold Time	0	–	–	ns
t_{DIS}	Output Disable Time	–	–	8	ns
t_{HLCH}	HOLD# Active Setup Time (relative to SCK)	3	–	–	ns
t_{CHHH}	HOLD# Active Hold Time (relative to SCK)	3	–	–	ns
t_{HHCH}	HOLD# Non Active Setup Time (relative to SCK)	3	–	–	ns
t_{CHHL}	HOLD# Non Active Hold Time (relative to SCK)	3	–	–	ns
t_{HZ}	HOLD# enable to Output Invalid	–	–	8	ns
t_{LZ}	HOLD# disable to Output Valid	–	–	8	ns
t_{WPS}	W#/ACC Setup Time (4)	20	–	–	ns
t_{WPH}	W#/ACC Hold Time (4)	100	–	–	ns
t_W	WRR Cycle Time	–	–	50	ms
t_{PP}	Page Programming (1)(2)	–	1.5	3	ms
t_{EP}	Page Programming (ACC = 9V) (1)(2)(3)	–	1.2	2.4	ms
t_{SE}	Sector Erase Time (64 kB) (1)(2)	–	0.5	2	sec
	Sector Erase Time (256 kB) (1)(2)	–	2	8	sec
t_{BE}	Bulk Erase Time (1)(2)(8)	–	128	256	sec
t_{PE}	Parameter Sector Erase Time (4 kB or 8 kB) (1)(2)	–	200	800	ms
t_{RES}	Deep Power-down to Standby Mode	–	–	30	µs
t_{DP}	Time to enter Deep Power-down Mode	–	–	10	µs
t_{VHH}	ACC Voltage Rise and Fall time	2.2	–	–	µs
t_{WC}	ACC at V_{HH} and V_{IL} or V_{IH} to first command	5	–	–	–

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, V_{CC} = 3.0V; 10,000 cycles; checkerboard data pattern.*
2. *Under worst-case conditions of 85°C; V_{CC} = 2.7V; 100,000 cycles.*
3. *Acceleration mode (9V ACC) only in Program mode, not Erase.*

4. *Only applicable as a constraint for WRR instruction when SRWD is set to a '1'.*
5. *t_{WH} + t_{WL} must be less than or equal to $1/f_C$.*
6. *∆ Full Vcc range (2.7 – 3.6V) and CL = 30 pF.*
7. *∞ Regulated Vcc range (3.0 – 3.6V) and CL = 30 pF.*
8. *Bulk Erase is on a die per die basis, not for the whole device.*
9. *When switching between die, a minimum time of t_{CS} must be kept between the rising edge of one chip select and the falling edge of the other for operations and data to be valid.*

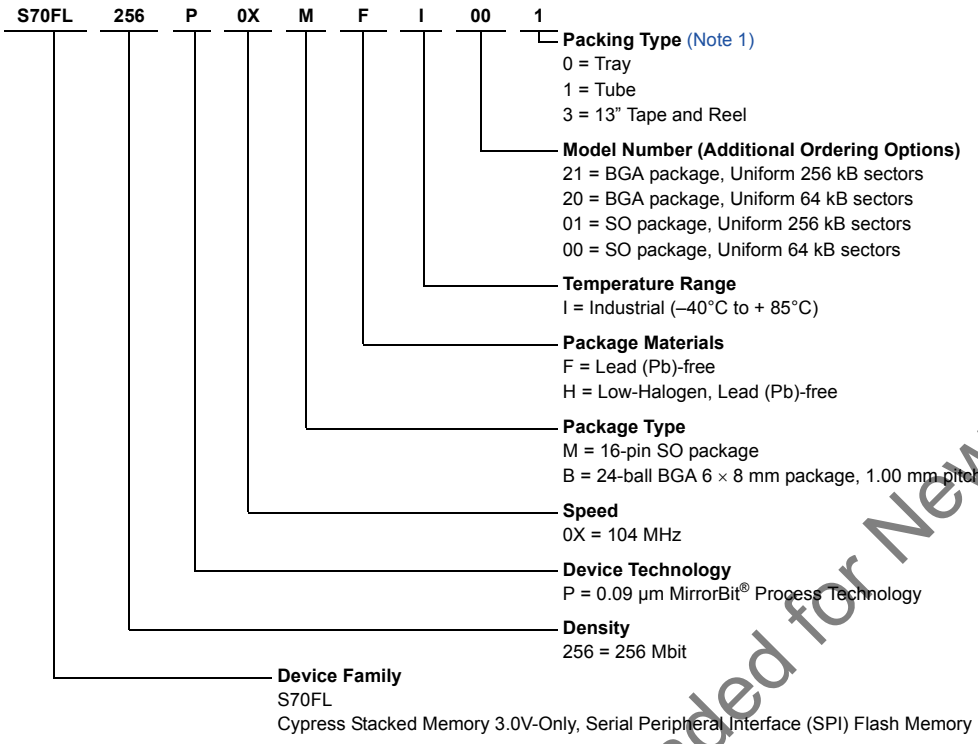
9.1 Capacitance

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance (applies to CS1#, CS2#, SCK, SI/IO0, SO/IO1, W#/ACC/IO2, HOLD#/IO3)	V_{OUT} = 0V	–	10.0	16.0	pF
C_{OUT}	Output Capacitance (applies to SI/IO0, SO/IO1, W#/ACC/IO2, HOLD#/IO3)	V_{IN} = 0V	–	22.0	30.0	pF

Notes:
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*
3. *For more information on pin capacitance, please consult the IBIS models.*

10. Ordering Information

The ordering part number is formed by a valid combination of the following:



10.1 Valid Combinations

Table 10.1 lists the valid combinations configurations planned to be supported in volume for this device.

Table 10.1 S70FL256P Valid Combinations Table

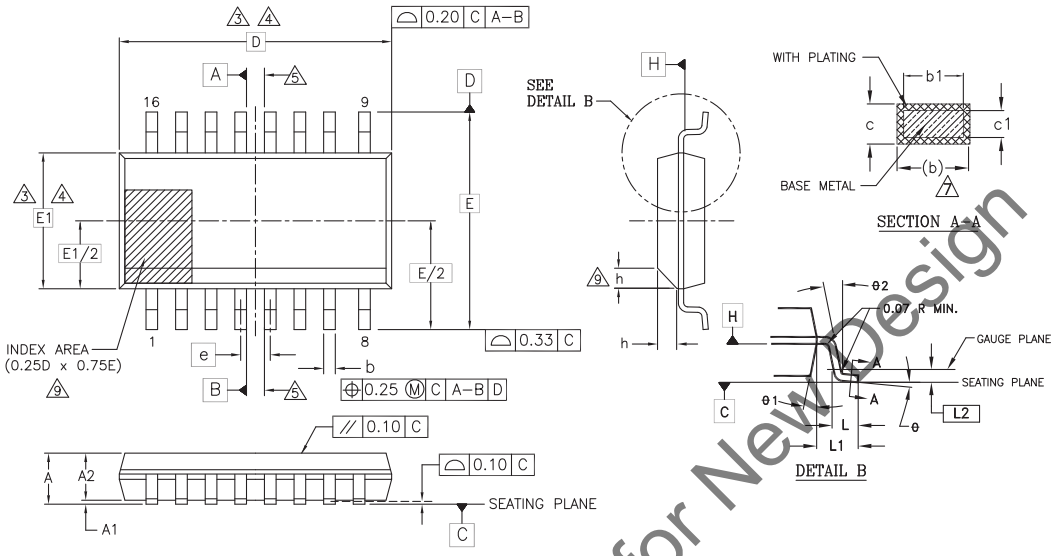
S70FL256P Valid Combinations					Package Marking
Base Ordering Part Number	Speed Option	Package and Temperature	Model Number	Packing Type	
S70FL256P	0X	MFI	00	0, 1, 3	70FL256P0XMFI00
			01		70FL256P0XMFI01
		BHI	20	0, 3	70FL256P0XBHI20
			21		70FL256P0XBHI21

Note:

1. Package Marking omits the leading "S70" and speed, package and model number.

11. Physical Dimensions

11.1 SL3 016 — 16-pin Wide Plastic Small Outline Package (300-mil Body Width)



PACKAGE	SL3016 (inches)		SL3016 (mm)	
JEDEC	MS-013(D)AA		MS-013(D)AA	
SYMBOL	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
A2	0.081	0.104	2.05	2.55
b	0.012	0.020	0.31	0.51
b1	0.011	0.019	0.27	0.48
c	0.008	0.013	0.20	0.33
c1	0.008	0.012	0.20	0.30
D	0.406 BSC		10.30 BSC	
E	0.406 BSC		10.30 BSC	
E1	0.295 BSC		7.50 BSC	
e	.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
L1	.055 REF		1.40 REF	
L2	.010 BSC		0.25 BSC	
N	16		16	
h	0.10	0.30	0.25	0.75
θ	0°	8°	0°	8°
θ1	5°	15°	5°	15°
θ2	0°		0°	

NOTES:

1. ALL DIMENSIONS ARE IN BOTH INCHES AND MILLMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH. BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

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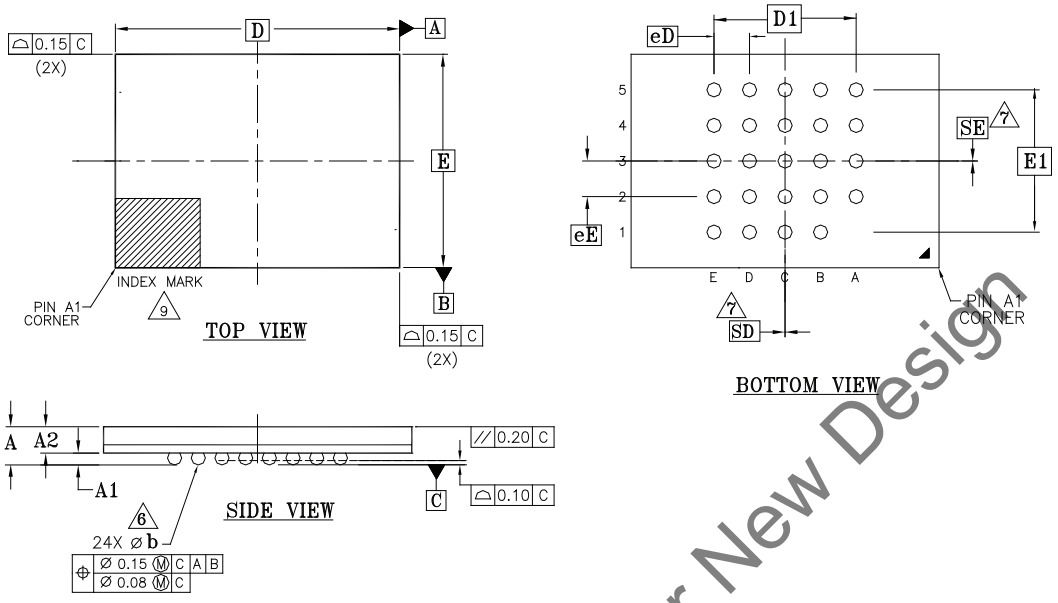
11.2 ZSA024 — 24-ball Ball Grid Array (6 × 8 mm) Package



PACKAGE	ZSA024			
JEDEC	N/A			
D x E	8.00 mm x 6.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.70	---	0.90	BODY THICKNESS
D		8.00 BSC.		BODY SIZE
E		6.00 BSC.		BODY SIZE
D1		4.00 BSC.		MATRIX FOOTPRINT
E1		4.00 BSC.		MATRIX FOOTPRINT
MD		5		MATRIX SIZE D DIRECTION
ME		5		MATRIX SIZE E DIRECTION
n		24		BALL COUNT
Øb	0.35	0.40	0.45	BALL DIAMETER
eE		1.00 BSC.		BALL PITCH
eD		1.00 BSC		BALL PITCH
SD / SE		0.00		SOLDER BALL PLACEMENT
		A1		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
   DATUM C IS THE SEATING PLANE AND IS DEFINED BY THE CROWNS OF THE SOLDER BALLS.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3645 16-038.86 Rev A \ 02.26.10

12. Revision History

Document History Page

Document Title: S70FL256P, 256-Mbit 3.0V Flash Document Number: 002-00647				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	BWHA	03/03/2010	Initial release
*A	–	BWHA	03/17/2010	Valid Combinations: Corrected Package Marking specification from discrete to MCP format Read Identification (RDID): Added section to explain CFI change from FL129P
*B	–	BWHA	06/17/2010	General: Changed product description from “256-Mbit CMOS 3.0 Volt Flash Memory with 93-MHz SPI Serial (Serial Peripheral Interface) Multi I/O Bus” to “256-Mbit CMOS 3.0 Volt Flash Memory with 104-MHz SPI Serial (Serial Peripheral Interface) Multi I/O Bus” Changed data sheet status from Advanced Information to Preliminary Distinctive Characteristics: Changed Normal READ clock rate from 36 to 40 MHz Changed FAST_READ maximum clock rate from 93 to 104 MHz Changed DUAL I/O FAST_READ clock rate from 72 to 80 MHz and effective data rate from18 to 20 MB/s Ordering Information: Changed description for Speed characters 0X from 93 to 104 MHz DC Characteristics: Changed I_{LI} (Input Leakage Current) value from ± 4 to ± 2 µA (max) Changed I_{LO} (Output Leakage Current) value from ± 4 to ± 2 µA (max) Changed I_{CC1} (Active Power Supply Current - READ) test condition frequencies from 72/93/36 MHz to 80/104/40 MHz Changed I_{CC1} (Active Power Supply Current - READ) value @ 80 MHz (dual/quad) from 41.8 to 44 mA (max) Changed I_{CC1} (Active Power Supply Current - READ) value @ 104 MHz (serial) from 27.5 to 32 mA (max) Changed I_{CC1} (Active Power Supply Current - READ) value @ 40 MHz (serial) from13.2 to 15 mA (max) Changed I_{CC2} (Active Power Supply Current - Page Program) value from 28.6 to 26 mA (max) Changed I_{CC3} (Active Power Supply Current - WRR) value from 16.5 to 15 mA (max) Changed I_{CC4} (Active Power Supply Current - SE) value from 28.6 to 26 mA (max) Changed I_{CC5} (Active Power Supply Current - BE) value from 28.6 to 26 mA (max) Added Note 2, clarifying that Bulk Erase is on a die per die basis, not for the whole device Test Conditions: Added note clarifying that input rise and fall times are 0-100%

Document History Page (Continued)

Document Title: S70FL256P, 256-Mbit 3.0V Flash Document Number: 002-00647				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*B (cont.)	–	BWHA	06/17/2010	AC Characteristics: Changed f_R (SCK Frequency for READ/RDID) values from 36/45 to 40/50 MHz (max) Changed f_C (SCK Frequency for others) values from 93/72 to 104/80 MHz (max) Changed t_V (Clock Low to Output Valid) values from 9.6/11.4/7.8/9.6 to 9/10.5/7.8/9 ns (max) Added t_{BE} (Bulk Erase Time) Added Note 8 clarifying that Bulk Erase is on a die per die basis, not for the whole device Added Note 9 clarifying that a minimum time of t_{CS} must be kept between the rising edge of one chip select and the falling edge of the other when switching between die for proper device functionality. Capacitance: Merged C_{IN} capacitance values into a single line item Merged Single I/O, Dual I/O, and Quad I/O max capacitance values into a single line item Added C_{IN} / C_{OUT} (Input / Output Capacitance) values of 6/8 pF (max) Added Notes clarifying test conditions
*C	–	BWHA	06/24/2011	Global: Promoted data sheet designation from Preliminary to Full Production
*D	–	BWHA	01/30/2013	Capacitance: Added “Typical” values column Corrected “Max” values for CIN / COUT (Input / Output Capacitance)
*E	4925834	BWHA	09/24/2015	Updated to Cypress template
*F	5155743	BWHA	03/10/2016	Added NRND note in page 1 specifying the suggested replacement parts. Updated General Description.

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